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| APPLICATION NO. | FILING DATE | FIRST NAMED INVENTOR | ATTORNEY DOCKET NO. | CONFIRMATION NO. |
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| 10/716,079 | 11/18/2003 | Jonghee Han | 2003P52882US | 4850 |

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| EXAMINER | |
|---|---|
| CHANG, DANIEL D | |

| ART UNIT | PAPER NUMBER |
|---|---|
| 2819 | |

DATE MAILED: 05/12/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

| Office Action Summary | Application No. | Applicant(s) | |
|---|---|---|---|
| | 10/716,079 | HAN, JONGHEE | |
| | Examiner | Art Unit | |
| | Daniel D. Chang | 2819 | |

*-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --*

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

1)☒ Responsive to communication(s) filed on *23 February 2006*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

4)☒ Claim(s) *2-5,8-19 and 22-27* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *25-27* is/are allowed.

6)☒ Claim(s) *2-5,8-15,17 and 22-24* is/are rejected.

7)☒ Claim(s) *16,18 and 19* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

**Application Papers**

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *11/23/05* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

### *Acknowledgement*

Receipt is acknowledged of the Amendment filed February 23, 2006.

### *Claim Rejections - 35 USC § 102*

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Claims 2-5, 8-15, 17, and 22-24 are rejected under 35 U.S.C. 102(e) as being anticipated by Kiehl (US 6,492,836 B2)

The applied reference has a common Assignee with the instant application. Based upon the earlier effective U.S. filing date of the reference, it constitutes prior art under 35 U.S.C. 102(e). This rejection under 35 U.S.C. 102(e) might be overcome either by a showing under 37 CFR 1.132 that any invention disclosed but not claimed in the reference was derived from the inventor of this application and is thus not the invention "by another," or by an appropriate showing under 37 CFR 1.131.

Regarding claim 2, Kiehl discloses, in Figs 2A-2C, a method of reducing skew between rising and falling data at an output node of a buffer circuit (200), comprising:

generating an intermediate voltage signal (220) from an input voltage signal applied to an input node (VIN) of the buffer circuit;

generating an output voltage signal at the output node (OUT) based on the intermediate voltage signal; and

coupling a first compensating current source (226, 230) between a supply voltage line and the output node to compensate (col. 5, lines 61+) for changes in NMOS current drive (see Fig. 2C), wherein the first compensating current source comprises a current source transistor (230) for delivering a compensating current (across 226) to the output node the current source transistor having a control terminal (gate of 230 connected to VIREFP) which is controlled independent (since signal at 220 and VIREFP are independent and separate signals; see col. 5, line 23 - col. 6, lines 64) on the intermediate voltage signal.

Regarding claim 3, Kiehl discloses, in Figs 2A-2C, coupling a second compensating current source (228, 232) between the output node and ground to compensate for changes in PMOS current drive.

Regarding claim 4, Kiehl discloses, in Figs 2A-2C, a method of reducing skew between rising and falling data at an output node of a buffer circuit (200), comprising:

generating an intermediate voltage signal (220) from an input voltage signal applied to an input node (VIN) of the buffer circuit;

generating an output voltage signal at the output node (OUT) based on the intermediate voltage signal;

coupling at least one compensating current source (230, 226/ 232, 228) to the output node to compensate for changes in at least one of a rate at which the output node is precharged (when 226 is on) and a rate at which the output node is discharged (when 228 is on); and

controlling the amount of current provided by the compensating current source via a process dependent current source whose current is mirrored by the compensating current (see Fig. 2C; col. 3, line 27-40; col. 5, lines 19-44).

Regarding claim 5, Kiehl discloses, in Figs 2A-2C, controlling the amount of current supplied by the compensating current source via a relatively process independent bias voltage applied to a gate of a transistor of the process dependent current source (col. 3, line 27-40; col. 5, lines 19-44; col. 5, lines 61+).

Regarding claim 8, Kiehl discloses, in Figs 2A-2C, a buffer circuit, comprising:

a first stage (202) for generating an intermediate voltage signal (220) from an input voltage signal applied to an input node (VIN) of the first stage;

a second stage (224) to receive the intermediate voltage signal and generate, on an output node of the second stage, an output voltage based on the intermediate voltage signal; and

at least a first compensating current source (226, 230) coupled to the output node to compensate (col. 5, lines 61+) for changes in at least one of a rate at which the output node is precharged and a rate at which the output node is discharged;

wherein the second stage comprises an inverter (225) formed by a PMOS transistor (251) and an NMOS transistor (253; see Fig. 2B) and wherein the first compensating current source comprises a first current source transistor (230) to supplement (via 226) current flowing into the output node through the PMOS transistor (251) as function of NMOS current drive (current driven by any of 232, 236, 253, and 228), the first current source transistor having a control terminal (gate of 230 connected to VIREFP) which is controlled independent (since signal at 220

and VIREFP are independent and separate signals; see col. 5, line 23 - col. 6, lines 64) on the intermediate voltage signal.

Regarding claim 9, Kiehl discloses, in Figs 2A-2C, that wherein changes in current provided by the first current source (230) are proportional (in some extent) to changes in current through the NMOS transistor (253 in 225).

Regarding claim 10, Kiehl discloses, in Figs 2A-2C, at least a second current source (228, 232) to supplement current flowing into the output node through the NMOS transistor (228) as function of PMOS current drive (current driven by any of 231, 234, 251, and 226).

Regarding claim 11, Kiehl discloses, in Figs 2A-2C, a buffer circuit, comprising:

a first stage (202) for generating an intermediate voltage signal (220) from an input voltage signal applied to an input node (VIN) of the first stage;

a second stage (224) to receive the intermediate voltage signal and generate, on an output node of the second stage, an output voltage based on the intermediate voltage signal; and

at least a first compensating current source (226, 230) coupled to the output node to compensate (col. 5, lines 61+) for changes in at least one of a rate at which the output node is precharged and a rate at which the output node is discharged;

wherein the second stage comprises an inverter (225) formed by a PMOS transistor (251) and an NMOS transistor (253) and the first compensating current source supplements current flowing from the output node through the NMOS transistor (253) as function of PMOS current drive (any of 231, 234, 251, and 226).

Regarding claim 12, Kiehl discloses, in Figs 2A-2C, that wherein changes in current provided by the first current source (226) are proportional to changes in current through the PMOS transistor (251 in 225).

Regarding claim 13, Kiehl discloses, in Figs 2A-2C, a buffer circuit, comprising:

a differential amplifier stage (202) for generating an intermediate voltage signal indicative of the voltage difference between a reference voltage signal and an input voltage signal applied to an input node of the differential amplifier stage;

an inverter stage (224) for generating, on an output node, an output voltage signal based on the intermediate voltage signal, wherein the inverter stage comprises at least one PMOS transistor (251) and at least one NMOS transistor (253); and

at least a first current mirror circuit (see circuit in Fig. 2C connected to 230 in Fig. 2A that forms a current mirror circuit) having a first branch (from Vdd to GND in Fig. 2C) and a second branch (Vdd to 244 via 230) coupled to the output node (via 226), the second branch delivering a current (via 226) to the output node, wherein current flowing through the first branch is dependent on changes in at least one of NMOS (current driven by NMOS transistor shown in Fig. 2C) or PMOS current drive (current driven by PMOS transistor shown in Fig. 2C) and current flowing through the second branch mirrors the current flowing through the first branch (inherent for a current mirror circuit).

Regarding claim 14, Kiehl discloses, in Figs 2A-2C, current flowing through the first branch of the first current mirror circuit varies with changes to the NMOS current drive (current driven by NMOS transistor shown in Fig. 2C); and

current flowing from the second branch of the first current mirror circuit supplements current flowing into the output node through the PMOS transistor (251).

Regarding claim 15, Kiehl discloses, in Figs 2A-2C, current flowing through the first branch of the first current mirror circuit varies with changes to the PMOS current drive (current driven by PMOS transistor shown in Fig. 2C); and

current flowing from the second branch of the first current mirror circuit supplements current flowing from the output node through the NMOS transistor (253).

Regarding claim 17, Kiehl discloses, in Figs 2A-2C, the current flowing through the first branch of the first current mirror circuit is set by a process independent bias voltage supplied to a gate of a process dependent transistor (col. 3, line 27-40; col. 5, lines 19-44; col. 5, lines 61+).

Claims 22-24 are similarly rejected as claims discussed above. As for the recitation, "memory device" and "an external clock signal", it has been held that a recitation with respect to the manner in which a claimed apparatus is intended to be employed does not differentiate the claimed apparatus from a prior art apparatus satisfying the claimed structural limitations. Ex parte Masham, 2 USPQ2d 1647 (1987).

## *Allowable Subject Matter*

Claims 25-27 are allowable over the prior art.

Claims 16, 18, and 19 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

The following is a statement of reasons for the indication of allowable subject matter: the

best prior art of record, Kiehl, taken alone or in combination of other references, does not teach or fairly suggest a buffer circuit comprising, among other things, at least a second current mirror circuit having a first branch and a second branch couple with the output node, wherein: current flowing though the first branch of the second current mirror circuit varies with changes to NMOS current drive: and current flowing from the second branch of the second current mirror circuit supplements current flowing into the output node through the PMOS transistor(claims 16 and 25); wherein the second branch of the first current mirror circuit comprises an NMOS transistor in parallel with the NMOS transistor of the inverter stage (claims 18 and 26); and wherein the second branch of the first current mirror circuit comprises an PMOS transistor in parallel with the PMOS transistor of the inverter stage (claims 19 and 27), as set forth in the claims.

***Response to Arguments***

Applicant's arguments filed 2/23/06 have been fully considered but they are not deemed to be persuasive.

Applicant merely argued on page 12 without any explanation that Kiehl does not teach a compensating current source that comprises a current source transistor for delivering a compensating current to the output node, the current source transistor having a control terminal which is controlled independent on the intermediate voltage sign, as claimed in independent claims 2, 8, and 22. Further, Applicant merely argued without any explanation that Kiehl does not teach "at least a first current mirror having a first branch and a second branch coupled to the output node, the second branch delivering a current to the output node," as claimed in

independent claim 13. Also, applicant merely argued without any explanation that Kiehl does not teach "coupling at least one compensating current source to the output node to compensate for changes in at least one of a rate at which the output node is precharged and a rate at which the output node is discharged; and controlling the amount of current provided by the compensating current source via a process dependent current source whose current is mirrored by the compensating current" as claimed in independent claim 4. Further, applicant merely argued without any explanation that Kiehl does not teach "at least a first compensating current source coupled to the output node to compensate for changes in at least one of a rate at which the output node is precharged and a rate at which the output node is discharged; and wherein the second stage comprises an inverter formed by a PMOS transistor and an NMOS transistor and the first compensating current source supplements current flowing from the output node through the NMOS transistor as function of PMOS current drive" as claimed in claim 11. However, as discussed above, Kiehl does teach all the features of the claimed invention. Therefore, the rejection is maintained as discussed above.

***Conclusion***

**THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

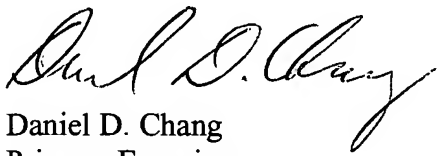
A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period

will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Daniel D. Chang whose telephone number is (571) 272-1801. The examiner can normally be reached on Monday through Friday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Rexford Barnie can be reached on (571) 272-7492. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).



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dc

**DANIEL CHANG**
**PRIMARY EXAMINER**